

**WHAT IS CLAIMED IS:**

- 1 1. A computer-implemented method for handling data using a  
2 plurality of processors, the method comprising:  
3 dividing a common memory, accessible to one or more  
4 first processors and to one or more secondary  
5 processors, into a plurality of data blocks using one  
6 of the first processors, the one or more first  
7 processors and the one or more second processors being  
8 chosen from a group of heterogeneous processors;  
9 identifying an available processor from the secondary  
10 processors to process one of the data blocks; and  
11 processing the data block using the available  
12 secondary processor.
- 1 2. The method of Claim 1, further comprising directly  
2 accessing the data block in the common memory using a  
3 memory access unit of the available secondary processor.
- 1 3. The method of Claim 2, further comprising transferring  
2 the data block using the available secondary processor  
3 from the common memory to a secondary memory local to the  
4 available secondary processor.
- 1 4. The method of Claim 3, further comprising transferring  
2 the data block using the available secondary processor  
3 from the secondary memory to the common memory after  
4 processing the data block.
- 1 5. The method of Claim 1, further comprising the available  
2 secondary processor notifying one of the first processors  
3 after processing the data block.

1 6. The method of Claim 1, further comprising requesting,  
2 using one of the first processors, the secondary  
3 processor to process the data block.

1 7. The method of Claim 1, wherein the dividing comprises  
2 dividing the common memory into data blocks, a size of  
3 the data blocks equaling a size of registers of the  
4 available secondary processor.

1 8. The method of Claim 1, further comprising processing the  
2 data block further using one of the first processors.

1 9. The method of Claim 1, further comprising identifying,  
2 using one of the first processors, additional available  
3 secondary processors to process data blocks until all the  
4 data blocks have been processed.

1 10. An information handling system comprising:

2 a plurality of heterogeneous processors, wherein the  
3 plurality of heterogeneous processors comprises one or  
4 more first processors and one or more secondary  
5 processors; and

6 a common memory accessible by the plurality of  
7 heterogeneous processors, wherein:

8 one of the first processors is adapted to divide the  
9 common memory into a plurality of data blocks,  
10 one of the first processors is adapted to identify  
11 an available processor from the secondary processors  
12 to process one of the data block; and  
13 one of the secondary processors is adapted to  
14 process the data block.

- 1 11. The information handling system of Claim 10, wherein the  
2 available secondary processor is further adapted to  
3 directly access the data block in the common memory using  
4 a memory access unit.
- 1 12. The information handling system of Claim 11, wherein the  
2 available secondary processor is further adapted to  
3 transfer the data block from the common memory to a  
4 secondary memory local to the available secondary  
5 processor.
- 1 13. The information handling system of Claim 12, wherein the  
2 available secondary processor is further adapted to  
3 transfer the data block from the secondary memory to the  
4 common memory after processing the data block.
- 1 14. The information handling system of Claim 10, wherein the  
2 available secondary processor is further adapted to  
3 notify one of the first processors after processing the  
4 data block.
- 1 15. The information handling system of Claim 10, wherein one  
2 of the first processors is adapted to request the  
3 available secondary processor to process the data block.
- 1 16. The information handling system of Claim 10, wherein the  
2 one first processor is further adapted to divide the  
3 common memory into data blocks, a size of the data blocks  
4 equaling a size of registers of one of the secondary  
5 processors.
- 1 17. The information handling system of Claim 10, wherein one  
2 of the first processors is adapted to further process the  
3 data block.

1 18. The information handling system of Claim 10, wherein one  
2 the first processors is adapted to identify additional  
3 available secondary processors to process data blocks  
4 until all the data blocks have been processed.

1 19. A computer program product on computer operable media,  
2 the computer program product comprising:

3 means for dividing a common memory, accessible to one  
4 or more first processors and to one or more secondary  
5 processors, into a plurality of data blocks, wherein  
6 the one or more first processors and the one or more  
7 second processors are selected from a group of  
8 heterogeneous processors;

9 means for identifying an available processor from the  
10 secondary processors to process one of the data  
11 blocks; and

12 means for processing the data block using the  
13 available secondary processor.

1 20. The computer product of Claim 19, further comprising  
2 means for directly accessing the data block in the common  
3 memory.

1 21. The computer product of Claim 20, further comprising  
2 means for transferring the data block from the common  
3 memory to a secondary memory local to the available  
4 secondary processor.

1 22. The computer product of Claim 21, further comprising  
2 means for transferring the data block from the secondary  
3 memory to the common memory after processing the data  
4 block.

- 1 23. The computer product of Claim 19, further comprising  
2 means for notifying one of the first processors after  
3 processing the data block.
- 1 24. The computer product of Claim 19, further comprising  
2 means for requesting the secondary processor to process  
3 the data block.
- 1 25. The computer product of Claim 19, wherein the means for  
2 dividing comprises means for dividing the common memory  
3 into data blocks, a size of the data blocks equaling a  
4 size of registers of the secondary processors.
- 1 26. The computer product of Claim 19, further comprising  
2 means for processing the data block further.
- 1 27. The computer product of Claim 19, further comprising  
2 means for identifying additional available secondary  
3 processors to process data blocks until all the data  
4 blocks have been processed.